REMARKS

Claims 1-8 have been amended. Claims 9-24 have been withdrawn as to a non-elected invention. Claims 1-24 remain pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and foregoing remarks.

Claims 1-6 stand rejected under 35 U.S.C. § 102(a) as being anticipated by the structure shown in Applicants' FIG. 1. The rejection is respectfully traversed.

The present invention relates to a semiconductor device with at least three wells formed in a semiconductor substrate. At least one well is formed to have a top surface height level higher than the top surface height levels of the *other two kinds of wells* in relation to the top surface of the semiconductor substrate. The prior art does not disclose such a structure.

FIGS. 1F and 1G illustrates a triple-well structure: lightly-N-well 5c, N-well 20 and P-wells 12. The thickness of oxide film 4c is *larger* than the thickness of oxide film 9 (FIG. 1(F)). After removing both of these oxide films, a difference in the height level of P-wells 12 and lightly-N-well 5c is generated. This is illustrated as element 13 in FIG. 1(G). This height difference may lead to wire-breaking in wiring of a polysilicon or metal which is formed over the step, *i.e.*, element 13 (Applicants' specification, p. 6, ll. 15-25). Applicants' claimed semiconductor, in contrast, avoids the step problem in the prior art.

One exemplary embodiment of Applicants' claimed structure is illustrated in FIG. 2. FIG. 2 illustrates that p-well 12 is formed in a p-type substrate 10. A lightly-doped n-well 5 is formed adjacent to p-well 12. A second n-well 20, having a greater

impurity concentration than the lightly-doped n-well 5 is formed on the opposite side of p-well 12. P-well 12 is formed to have a surface level (height) *higher than the surface* level of lightly-doped n-well 5 and n-well 20. The step level difference between wells 5, 20, and 12 is small compared to the prior art.

In the prior art, the step level difference between p-well 12 and lightly-doped n-well 5c was large, and lightly-doped n-well 5c possessed a different step level than n-well 20. Applicants' claimed structure, in contrast, does *not* have two different step levels (FIG. 2). Light-doped n-well 5c and n-well 20 have substantially the same surface height levels with respect to each other (Applicants' specification, p. 21, ll. 2-10). The prior art has three types of wells having "*gentle two steps*," as discussed on page 7, lines 1-18 of the specification, and does not produce one kind of well with a higher surface height level than two other kinds of wells having substantially the same top surface height as each other.

Nonetheless, claim 1 now recites, as amended, that the "other two kinds of wells have substantially the same top surface height level as each other." As indicated above, the prior art does *not* have such features. In FIG. 1(G), N-well 20 and lightly-N-well 5c, and p-wells 12 all have *different* top surface height levels with respect to each other.

Claims 2-6 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above, and on their own merits.

Claims 7-8 depend from claim 1 and should be similarly allowable along with claim 1 for at least the reasons provided above, and on their own merits. Please note that Hirase is relied upon for disclosing a three-well MOS transistor structure formed

by a drain diffusion layer and a source diffusion layer, and adds nothing to rectify the deficiencies associated with the prior art discussed above.

Moreover, Applicants respectfully submit that Hirase does *not* teach or suggest a semiconductor device comprising, *inter alia*, "at least three kinds of wells formed in and on a top surface of [a] substrate, wherein at least one kind of well has a top surface height level higher than the top surface height levels of the other two," as recited in claim 1. All of the wells in Hirase are the *same height* as each other.

For example, Hirase FIGS. 1 and 4 illustrates p-wells 4 and 5 that are electrically isolated from each other. N-wells 6a, 6b, and 6c are formed adjacent to p-wells 4 and 5. Underneath n-well 6a is formed a deep buried well 3a. Underneath p-well 5, a deep p-well 7 is formed. Underneath n-wells 6b and 6c, a buried deep n-well 3b is formed. The buried deep n-well 3b isolates p-well 4 from substrate 1. However, all of Hirase's wells 4, 5, and 6a-6c are formed to have the *same top surface height levels* (FIGS. 1 and 4).

Consequently, the proposed combination involving Hirase would still *not* yield a structure with "other two kinds of wells [having] *substantially the same top surface height level* as each other," as recited in claim 1 (emphasis added). These are additional reasons for the allowance of dependent claims 7 and 8.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

Dated: November 8, 2005

Respectfully submitted,

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